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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 23/64, 21/31 // 21/306, 21/762, H01F 5/00 — A1

(11) International Publication Number: WO 97/45873

(43) International Publication Date: 4 December 1997 (04.12.97)

(21) International Application Number: PCT/SE97/00954

(22) International Filing Date: 30 May 1997 (30.05.97)

(30) Priority Data:
9602191-0 31 May 1996 (31.05.96) SE

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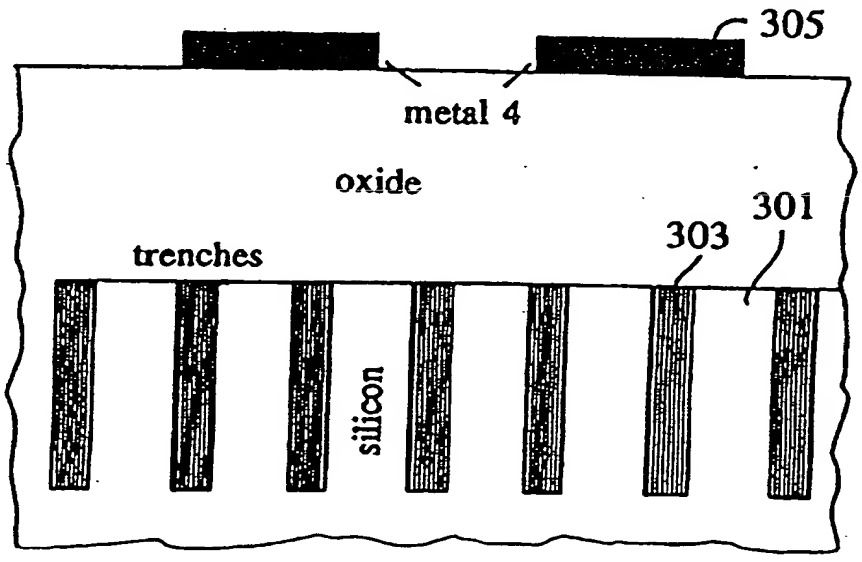
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BI BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GI GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LI LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT UA, UG, UZ, VN, YU, ARIPO patent (GH, KE, LS, MW SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MI RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patei (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TI TG).

Published
With international search report.

(54) Title: CONDUCTORS FOR INTEGRATED CIRCUITS



(57) Abstract

The quality factor (Q-value) of spiral inductors or coils (305) in IC-circuits is improved by partially removing the semiconducting substrate (301) under the inductor (305) by etching trenches (303), which are refilled with an isolating material. Hence, the losses caused by the substrate (301) are reduced and the quality factor is increased accordingly. The parasitic capacitance to the substrate (301) is also reduced, increasing the resonance frequency of the inductor (305) and extending the useful frequency range of operation of the inductor. Furthermore, by utilizing the uppermost metals of a multi-layer metal structure in the circuit, additional reduction of losses and parasitic capacitance are also achieved. The use of trenches (303) under metal patterns for loss and capacitance reduction is not limited to spiral inductor layouts, and can be used for any metal line, bond pad, etc.

CONDUCTORS FOR INTEGRATED CIRCUITS

TECHNICAL FIELD

The present invention relates to an electrical conductor in an integrated circuit (IC) having a low loss to a substrate and a method of making such a conductor, in particular to a method of fabricating spiral inductors and also to an integrated circuit inductor.

BACKGROUND OF THE INVENTION

Advanced silicon bipolar, CMOS and BiCMOS circuits are today used for high-speed electronic applications in the 1 - 2 GHz frequency range and they replace circuits previously only possible to implement using devices based on materials found in column III-V in the periodic table.

Inductor elements are often needed in high-frequency circuits when forming blocks like resonators and filters. A problem common to all integrated circuit devices is how to achieve integrated circuit inductors having high quality factors, Q, and high operating frequencies, the operating frequency being limited by the resonance frequency.

The quality factor, Q-value, is the ratio of the stored energy to the loss energy and can be computed for an inductor as $Q = 2*\pi*f*L/R$, where f is the operation frequency, L the inductance and R is the resistive losses of the metal, not taking any parasitic losses from an underlying substrate into account.

Because of the conducting properties of the substrate, the Q-value of the inductor is reduced. By selectively removing the silicon under the inductor, higher Q-values and higher resonance frequencies are obtained. The Q-value can be increased by a factor of two by such a removal. The removal can be in the form of a silicon etching process, giving air gaps of several hundred micrometers, see J.Y.C. Chang, A.A. Abidi, M. Gaitan, "Large Suspended Inductor on Silicon and Their Use in a 2 μm CMOS RF Amplifier", IEEE Transactions on Electron Devices Vol. 40, No. 5, p. 246, May 1993, but such removals are not regarded as feasible in large production volumes or compatible with silicon

A better way of reducing the resistance is to make an inductor having parallel spiral paths in adjacent layers, e.g. to connect the uppermost metal layers in parallel. The Q-value of the inductor can in this way be increased 1.5 - 2 times, at the expense of a lower resonance frequency because of the decreased isolation thickness. By increasing the number of turns of the spiral, the inductance value is made larger. The capacitance of the inductor spiral to the substrate will however also increase, leading to a lower resonance frequency limiting the useful frequency range of operation of the inductor.

Thus U.S. patent 5,446,311 describes such a structure having an inductor formed in multiple metal layer levels in order to reduce the inductor resistance.

Furthermore, the Japanese patent application JP A 07-106 514 discloses a structure similar to the structure described in U.S. patent 5,446,311, in which the loss due to electrostatic capacity is reduced and the Q-value is increased by forming an inductor which has two spiral metallic paths formed in different metallization layers and which are interconnected by a third layer.

Deep trenches are applied in modern IC processes for isolation of devices. The advantages of such trenches are reduced parasitic capacitances and reduced device spacing. A deep, 5 - 20 μm, and narrow, 1 - 2 μm, trench is obtained by means of dry etching and refilling it with oxide and undoped poly-silicon or a dielectric material. After the refilling process, the surface of the substrate will be coated with a layer of refilling material and thus be substantially flat so that e.g. metal layers can be placed over the trenches without any restrictions.

Also, in U.S. patents 5,336,921 and 5,372,967 a method of forming an inductor in a vertical trench is described. The inductor described aims at eliminating some of the problems encountered with conventional, horizontal inductors on integrated circuits by means of providing a method of fabricating vertical inductors in the shape of an inductive coil in a trench.

Trenches can also be used under any metal line or bond pad in order to reduce parasitic capacitance and reduce losses to the substrate.

In addition, no process changes or additional process steps are necessary to achieve this if an advanced Si-IC process is used.

Thus in a method of fabricating an integrated circuit inductor or an integrated circuit comprising an inductor the inductor is produced in or on an electrically semiconducting or semi-isolating substrate and in particular by depositing or coating various layers on a silicon substrate. The inductor can generally comprise a structure of electrical conductor paths extending substantially in one plane or in several, for example substantially parallel planes. Before the conductor paths are produced, in particular before the inductor metal paths are applied to or deposited on the substrate, trenches are etched in the substrate extending from the substrate surface at suitable locations. The locations of the trenches are selected so that the inductor paths will be located above and close to the trenches and generally so that the trenches will intersect the hypothetical electrical current paths inside the material of the substrate, when the inductor is used and there is an electrical current flowing therein and no trenches would have been made in the substrate, this configuration of the trenches then attenuating or hindering the currents inside the substrate. The trenches are filled with an electrically isolating material, in particular a dielectric or semiconducting material, in order that the following process steps when making the conductor paths will experience a substantially flat surface.

The trenches may then advantageously be arranged so that they occupy the largest possible area under the inductor, that is they can be densely spaced. Also, the trenches are preferably arranged in a structure of substantially parallel trenches or a in meshlike structure.

The integrated circuit having an inductor integrated therein thus comprises, in the most general aspect, thin plates of a

An integrated circuit can as above, generally, comprise a metal conductor formed on or in an electrically semiconducting or semi-isolating substrate, in particular on a silicon substrate, the conductor for example being a part of an inductor path. Also, then, plates or trenches can be arranged in a region or region adjacent the conductor as described above, for reducing losses in the conductor to the substrate. The plates can then as above for example be arranged substantially perpendicularly to the plane of the conductor or the electrical current path therein. The plates may be filled trenches arranged to generally cross the electrical current path in the metallic conductor and preferably to extend in a direction substantially perpendicular to said current path and/or in a longitudinal direction of the conductor.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described in greater detail with reference to the accompanying drawings, in which:

- Fig. 1 is a highly schematic, rectangular spiral layout as seen from above for an integrated circuit inductor according to state of the art,
- Fig. 2a and 2b are schematic cross sectional views of the inductor in fig. 1,
- Fig. 3 is a schematic cross sectional view of an integrated circuit inductor,
- Fig. 4 is a trench pattern to be used on a substrate,
- Fig. 5 shows a trench pattern under a metal conductor line.

DESCRIPTION OF A PREFERRED EMBODIMENT

In fig. 1 a state of the art rectangular spiral layout forming an inductor is shown. The inductor is in this case formed in a fourth, as mounted bottom up, uppermost metal layer 101 by a spiral, electrically conductive path comprising a number of rectangular turns, the number of turns typically being between 5 and 10. A lower metallization layer 103, in this case the third layer, is used for closing the spiral structure by means of a cross-under.

The inductor structure of fig. 1 is also shown in cross section-

etching and refilling the etched voids with an isolating material like silicon oxide and undoped poly-silicon or a dielectric material. The surface above the substrate produced in the refilling process will then still be substantially flat. The trenches can have widths of about 1 - 2 μm and depths of about 5 - 20 μm. The width of the substrate material between neighbouring trenches may be as small as is practically possible, for instance 2 - 4 μm. The trenches are arranged in some suitable pattern to cross the overlying conductor paths.

Fig. 4 shows a view of a portion of a substrate 401 from above in which a preferred pattern of trenches 403 has been etched. The trench pattern is then used under an inductor for reducing the losses to the substrate. The pattern comprises a first set of several straight identical trenches located in parallel to each other and having an equal spacing and also a second set of identical trenches located in parallel to each other and equally spaced, the trenches of the second set being perpendicular to those of the first set. The trenches should always be so long and located that they pass beyond the outermost inductor turn into the free material surrounding the inductor. The trench pattern used can however have any meshlike shape, and it is generally desirable to remove as much of the substrate as possible.

Finally, fig. 5 shows how the method as described herein can be used in another application. In this case trenches 501 are etched under a metallization line 503 in order to reduce the parasitic capacitance and reduce losses to the substrate. The trenches may have the same dimensions as discussed above and they are arranged to cross under the electrically conductive path at substantially straight angles. They can be located symmetrically under the conductor path and extend to each side of the path as long as is required or possible, e.g. some 4 - 10 μm. This trench configuration or preferably the meshlike configuration of fig. 3 can be also used for reducing losses of bond pads.

longitudinal directions of the trenches are arranged to cross the electrical current path in the metallic conductor, in particular to extend in a direction substantially perpendicular to said path and/or to a longitudinal direction of the conductor.

6. An inductor in an integrated circuit formed on or in an electrically semiconducting or semi-isolating substrate, in particular on a silicon substrate, and comprising a structure of conductor paths extending in one plane or a plurality of substantially parallel planes, characterized by thin plates of a material being a worse or poorer electrical conductor than the substrate, which are arranged in the substrate in a region at the conductor paths, the plates in particular being trenches in the substrate located under the inductor paths and refilled with an electrically isolating material, in particular a dielectric or semiconducting material.

7. An inductor according to claim 6, characterized in that the plates are arranged substantially perpendicularly to the plane or planes of the conductor paths.

8. An inductor according to any of claims 6 or 7, characterized in that the plates are arranged substantially in parallel to each other.

9. An inductor according to any of claims 6 - 8, characterized in that the width of the plates is substantially equal to the width of the conductor paths.

10. An inductor according to any of claims 6 - 9, characterized in that the plates are densely arranged, so that the interspace between neighbouring trenches is small, preferably substantially equal to 2 or a few times the width of the trenches.

11. An inductor according to any of claims 6 - 10, characterized in that the plates are arranged in a meshlike structure.

12. A method of fabricating an integrated circuit inductor in or

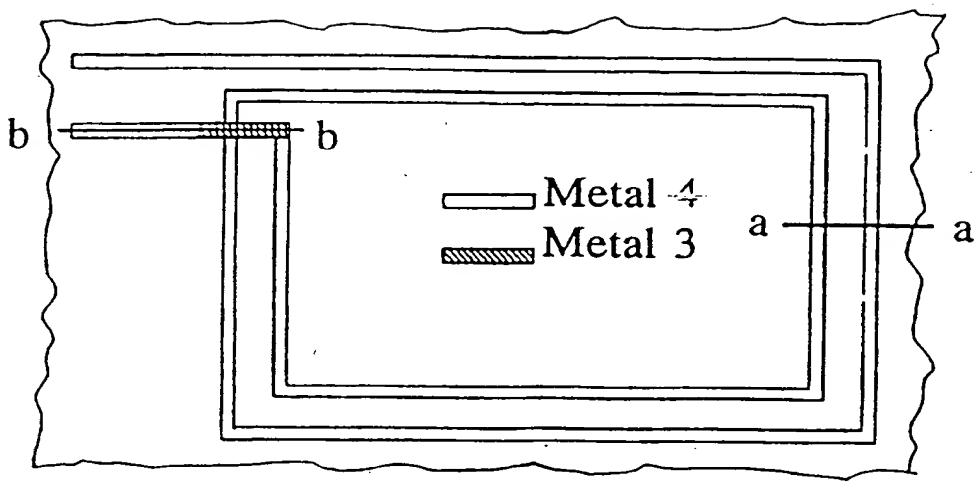


Fig. 1

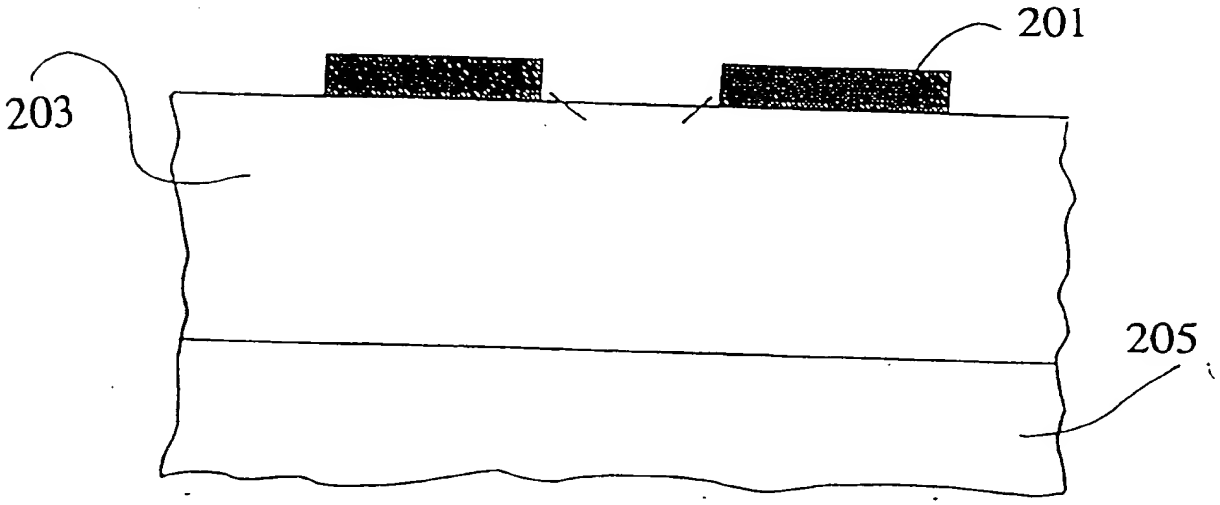


Fig. 2a

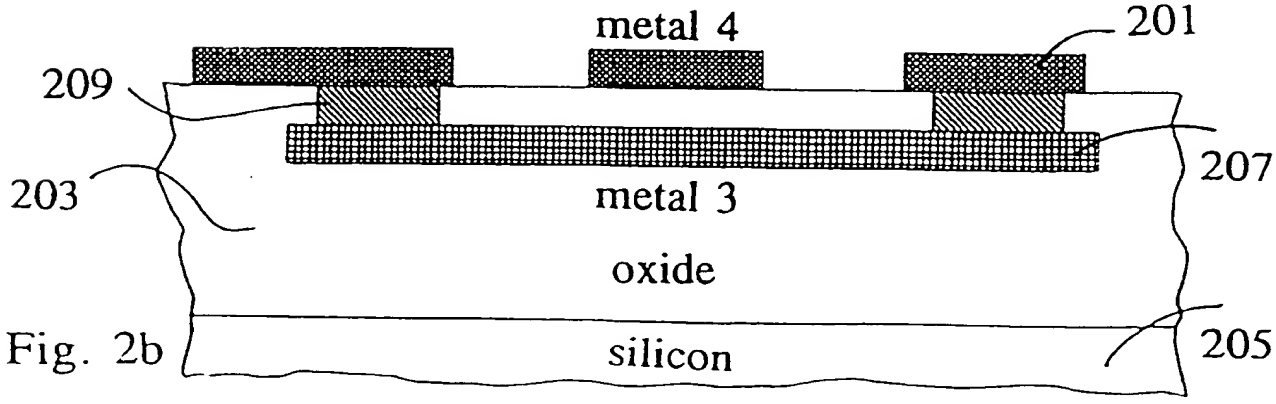


Fig. 2b

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 97/00954

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 23/64, H01L 21/31 // H01L 21/306, H01L 21/762, H01F 5/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 9417558 A1 (THE REGENTS OF THE UNIVERSITY OF CALIFORNIA), 4 August 1994 (04.08.94), column 3, line 16 - line 24, figure 2	1,2,5-9
A	--	3,4,10-14
Y	US 5095357 A (NAOTO ANDOH ET AL), 10 March 1992 (10.03.92), column 1, line 41 - line 45; column 5, line 37 - line 40, figure 4	1,2,5-9
A	--	3,4,10-14

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" erlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 Sept 1997	12.09.97
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Pär Moritz Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

Information on patent family members

06/08/97

International application No.
PCT/SE 97/00954

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		EP 0643403 A,B	15/03/95
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